11-29-00

A

FISH & RICHARDSON P.C.

225 Franklin Street
Boston, Massachusetts
02110-2804

Telephone
617 542-5070

Facsimile
617 542-8906

Web Site
www.fr.com

Frederick P. Fish
1855-1930

W.K. Richardson
1859-1951

November 28, 2000

Attorney Docket No.: 12407-004001

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Commissioner for Patents
Washington, DC 20231

Presented for filing is a new original patent application of:

Applicant: JOHN REDFORD

Title: BRANCH HANDLING FOR SINGLE INSTRUCTION MULTIPLE DATAPATH PROCESSOR ARCHITECTURES

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Enclosed are the following papers, including those required to receive a filing date under 37 CFR §1.53(b):

	Pages
Specification	6
Claims	3
Abstract	1
Declaration (unsigned)	1
Drawings	2

Enclosures:
— Postcard.

This application is entitled to small entity status. A small entity statement will be filed at a later date.

CERTIFICATE OF MAILING BY EXPRESS MAIL

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6

Basic filing fee	$355
Total claims in excess of 20 times $9	$0
Independent claims in excess of 3 times $40	$40
Fee for multiple dependent claims	$0
Total filing fee:	$395

A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (617) 542-5070.

Kindly acknowledge receipt of this application by returning the enclosed postcard.

Please send all correspondence to:

PETER J. DEVLIN
Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804

Respectfully submitted,

Peter J. Devlin
Reg. No. 31,753
Enclosures
PJD/lxm
20153182 doc

Attorney's Docket No.: 12407-004001

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: BRANCH HANDLING FOR SINGLE INSTRUCTION MULTIPLE DATAPATH PROCESSOR ARCHITECTURES

APPLICANT: JOHN REDFORD

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BRANCH HANDLING FOR SINGLE INSTRUCTION MULTIPLE DATAPATH PROCESSOR ARCHITECTURES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to a copending application entitled HANDLING CONDITIONAL PROCESSING IN A SINGLE INSTRUCTION MULTIPLE DATAPATH PROCESSOR ARCHITECTURE, which was filed on the same day as this application and is incorporated herein by reference.

TECHNICAL FIELD

This invention relates to handling conditional processing in a single instruction multiple datapath (SIMD) processor architecture.

BACKGROUND

Parallel processing is an efficient way of processing an array of data items. A SIMD processor is a parallel processor array architecture wherein multiple datapaths are controlled by a single instruction. Each datapath handles one data item at a given time. In a simple example, in a SIMD processor having four datapaths, each data item in a four data item array would be processed in a respective one of the four datapaths.

During program execution in the SIMD processor, multiple datapaths may be enabled prior to encountering a conditional processing block, such as an if-then-else-processing block. Before executing the conditional processing block, the processor enable (PE) states of each of the datapaths, i.e., whether they are enabled or disabled, must be saved in case any of the datapath PE states is changed during execution of the conditional processing block. Further, upon exiting the conditional processing block, the PE states of the datapaths must be restored to the states that existed prior to entry of the conditional processing block.

SUMMARY

In a general aspect, the invention features a method of determining whether datapaths executing a computer program should execute conditional processing in the computer program. The method includes determining whether PE states of all of the datapaths are disabled, and branching around the conditional processing if the PE states of all of the

datapaths are disabled. Instructions are also provided for performing the determining and the branching.

In a preferred embodiment, branching is not performed if the program is determined to be deterministic.

The determination of whether the PE states of all of the datapaths are disabled includes evaluating a processor enable bit associated with each one of the datapaths. The processor enable bit is enabled if it is a value of one. The processor enable bit is disabled if it is a value of zero.

The determination of whether the computer program is deterministic includes evaluating a deterministic bit. The deterministic bit is a first value to indicate that the computer program is deterministic, and is a second value to indicate that the computer program is non-deterministic.

In another aspect, the invention features instructions that combine the branching with operations that maintain the PE states during the conditional processing. One such instruction causes the datapaths to establish a state of the datapaths' PE states for the conditional processing, determine whether the established PE states are all disabled, and branch around the conditional processing if the established PE states of all of the datapaths are disabled.

The conditional processing is, e.g., an if-processing block, and in this case the instructions also cause the datapaths to save a current state of the PE states prior to establishing them for the conditional processing. The conditional processing may also include an else-processing block.

Embodiments of various aspects of the invention may have one or more of the following advantages.

If all datapaths are disabled prior to entering an if-processing block or an else-processing block, there is no work to be accomplished in these blocks. Therefore, branching around the work allows the program to run faster. Combining the branching operation with operations that maintain the PE states during conditional processing provides faster, more efficient program execution, and simpler programming.

Testing a deterministic indicator provides a manner of overriding the branching in program code that must meet real time deadlines.

Other features and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a block diagram of a single instruction multiple datapath (SIMD) processor.

FIG. 2 is a block diagram of a program having branch processes for skipping conditional processing in some situations.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Referring to FIG. 1, a single instruction multiple datapath (SIMD) processor 10 includes an instruction cache 12, control logic 14, a serial datapath 16, and a number of parallel datapaths labeled 18a, 18b, 18c, 18, ... 18n. The parallel datapaths 18 write to a memory 20. Each of the datapaths 18 has an associated processor enable (PE) bit 22 that represents the PE state of that datapath. Specifically, parallel datapath 18a is associated with a PE bit 22a, parallel datapath 18b is associated with a PE bit 22b, and so forth. When a PE bit is enabled, its associated parallel datapath is enabled and data items may be written by that parallel datapath. For example, if PE bit 22a is enabled, data items may be written by parallel datapath 18a; if PE bit 22b is enabled, data items may be written by parallel datapath 18b. If PE bit 22n is enabled, data items may be written by parallel datapath 18n. When a PE bit is disabled, its associated parallel datapath is disabled and data items may not be written by that parallel datapath.

In operation, the control logic 14 fetches an instruction from the instruction cache 12. The instruction is fed to the serial datapath 16 that provides the instruction to the datapaths 18. Each of the datapaths 18 is read together and written together unless the processor enable bit is disabled for a particular datapath.

When an instruction causes the SIMD processor 10 to execute a conditional processing block within the program code (e.g., a processing block that includes one or more if-then-else processing statements), the current PE state of each of the datapaths must be accounted for, so that if any of the PE states of the datapaths are altered during execution of the conditional processing block, the PE states can be restored upon the completion of the conditional processing block. Often, a conditional processing block contains multiple

conditional processing operations, some of which may be executed during (i.e., nested within) the processing of other conditional processing operations. In order to assure proper operation, the PE state of each datapath must be saved prior to entering each nested conditional operation, and the saved PE state must be restored upon completing the conditional operation.

Referring to Fig. 2, program code 40 that contains a conditional processing block 42 is shown. Conditional processing block 42 is an if-then-else processing block in this example, and thus includes an if-processing block 44 followed by an else-processing block 46. It will be understood that program code 40 may contain many other conditional processing blocks 42, and indeed, conditional processing block may include additional if-processing blocks 44 and/or else-processing blocks 46 nested within it. A single conditional processing block with one if-processing block 44 and one else-processing block 46 is shown merely for simplicity in describing an embodiment of the invention.

At the start of if-processing block 44, the current PE states of datapaths 18 are saved, and an if-processing statement is executed. The PE states of datapaths 18 are then set to either the enable state (PE=1) or the disable state (PE=0) according to the results of the if-processing statement. Only those datapaths having an enabled PE state will perform subsequent processing in if-processing block 44. Accordingly, if all datapaths 18 are set to the disabled PE state, no processing work will be performed within if-processing block 44.

Branch process 50 is inserted in program code 40 at the start of if-processing block 44. Branch process 50 tests the PE states of datapaths 18 upon the execution of the if-processing statement. If all datapaths are disabled (i.e., PE=0), the processing operation in if-processing block 44 may be skipped without affecting the computational results of program 40. Accordingly, branch process 50 branches 52 around if-processing block 44 to else-processing block 46.

The PE states of datapaths 18 are also tested at the start of else-processing block 46. If all datapaths 18 are disabled (i.e., PE=0), no processing work will be performed within else-processing block 46. Accordingly, branch process 60 branches 62 around else-processing block 46 to, in this example, the end 64 of conditional processing block 40.

In some cases, the execution of program 40 is deterministic. That is, for one reason or another (such as to meet real-time deadlines), it is desirable to execute program 40 in the

same amount of time regardless of whether any work in the program (such as if-processing block 44 and/or else-processing block 46) could be skipped. If so, a deterministic bit (DET, Fig. 1) is set by the programmer in a control register of SIMD processor 10. Branch processes 50, 60 test the state (0 or 1) of the DET bit and do not branch 52, 62 if the DET bit is set.

The copending application describes methods of saving and maintaining the PE states of datapaths 18 during conditional processing, such as if-then-else processing. Branch processes 50, 60 combine the branching determination with the PE state setting and maintaining operations, to provide instructions that respectively handle all of the work needed for an if-processing statement and an else-processing statement.

Branch process 50 combines the PE state saving operation with the branching operation, and is of the following form:

if (SAVE_PE (Px), PE = Pn =0) go to X

Branch process 50 saves the PE state of the datapaths in register Px, and then sets the PE state equal to the contents of register Pn. If those contents are 0 (i.e., if none of the datapaths' PE bits are set), branch process 50 branches 52 to destination X (e.g., the subsequent else-processing block 46).

As described in the copending application, a datapath's PE state is, under some conditions, inverted (i.e., from 0 to 1 or 1 to 0) prior to an else-processing block. The instruction for doing so is called a "FLIP" instruction in the copending application. Branch process 60 combines the FLIP instruction with the branching operation, and is of the following form:

if (FLIP_PE (Px)) go to Y

Branch process 60 will invert the appropriate PE bits (according to the rules described in the copending application) and will branch to destination Y (i.e., the end 64 of else-processing block 46) if none of the PE bits are set.

Other embodiments are within the scope of the following claims.

For example, branch processes 50, 60 may be used with other instructions that save and manipulate PE states during conditional processing.

Another branch process may be inserted at the start of conditional processing block 42 to determine whether the current PE states of all datapaths 18 (i.e. the PE states prior to

performing any conditional processing statement) are disabled. If all PE states are disabled, none of datapaths 18 will perform either if-processing block 44 or else-processing block 46. Accordingly, this branch process will branch around the entire conditional processing block 42. As with branch processes 50, 60, branching is not performed if the deterministic bet DET is set.

Embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method of determining whether a plurality of datapaths executing a computer program should execute conditional processing in the computer program, comprising:

determining whether PE states of all of the datapaths are disabled;

determining whether the computer program is deterministic; and

branching around the conditional processing if the PE states of all of the datapaths are disabled and the computer program is non-deterministic.

2. The method of claim 1 wherein determining whether the PE states of all of the plurality of datapaths are disabled comprises:

evaluating a processor enable bit associated with each one of the plurality of datapaths.

3. The method of claim 2 wherein the processor enable bit is enabled if it is a value of one.

4. The method of claim 2 wherein the processor enable bit is disabled if it is a value of zero.

5. The method of claim 1 wherein the determining of whether the computer program is deterministic comprises evaluating a deterministic bit.

6. The method of claim 5 wherein the deterministic bit contains a first value indicating the computer program is deterministic.

7. The method of claim 5 wherein the deterministic bit contains a second value indicating the computer program is non-deterministic.

8. A method of determining whether a plurality of datapaths executing in a program should execute a conditional processing block in the program comprising:

determining whether all PE states of the datapaths are disabled; and

branching around the conditional processing block if the PE states of all the datapaths are disabled.

9. The method of claim 8 wherein determining further comprises:

determining whether the program is non-deterministic.

10. The method of claim 9 wherein the branching further comprises:

branching if the PE states of all of the datapaths are disabled and the program is non-deterministic.

11. The method of claim 9 further comprising not branching if the program is deterministic.

12. An instruction set executed by datapaths during conditional processing, comprising an instruction that causes the datapaths to

determine whether PE states of all of the datapaths are disabled, and

branch around the conditional processing if the PE states of all of the datapaths are disabled.

13. The instruction set of claim 12 wherein the branching is not performed if the program is deterministic.

14. An instruction set executed by datapaths during conditional processing, comprising an instruction that causes the datapaths to

establish a state of PE states of the datapaths for the conditional processing,

determine whether the established PE states of all of the datapaths are disabled, and

branch around the conditional processing if the established PE states of all of the datapaths are disabled.

15. The instruction set of claim 14 wherein the conditional processing includes an if-processing block.

16. The instruction set of claim 15 wherein the instruction further causes the datapaths to save a current state of the PE states prior to the establishing

17. The instruction set of claim 14 wherein the conditional processing includes an else-processing block.

18. The instruction set of claim 14 wherein the branching is not performed if the program is deterministic.

ABSTRACT

A method of determining whether datapaths executing in a computer program should execute conditional processing block includes determining whether processor enable (PE) states of all of the datapaths are disabled, and branching around the conditional processing if the PE states of all of the datapaths are disabled. Branching is not performed, even if the PE states of all of the datapaths are disabled, if the program is determined to be deterministic. That determination is made by evaluating the state of a deterministic bit. Instructions are also provided for carrying out the determining and branching operations. The instructions may also be combined with operations that maintain the PE states during conditional processing.

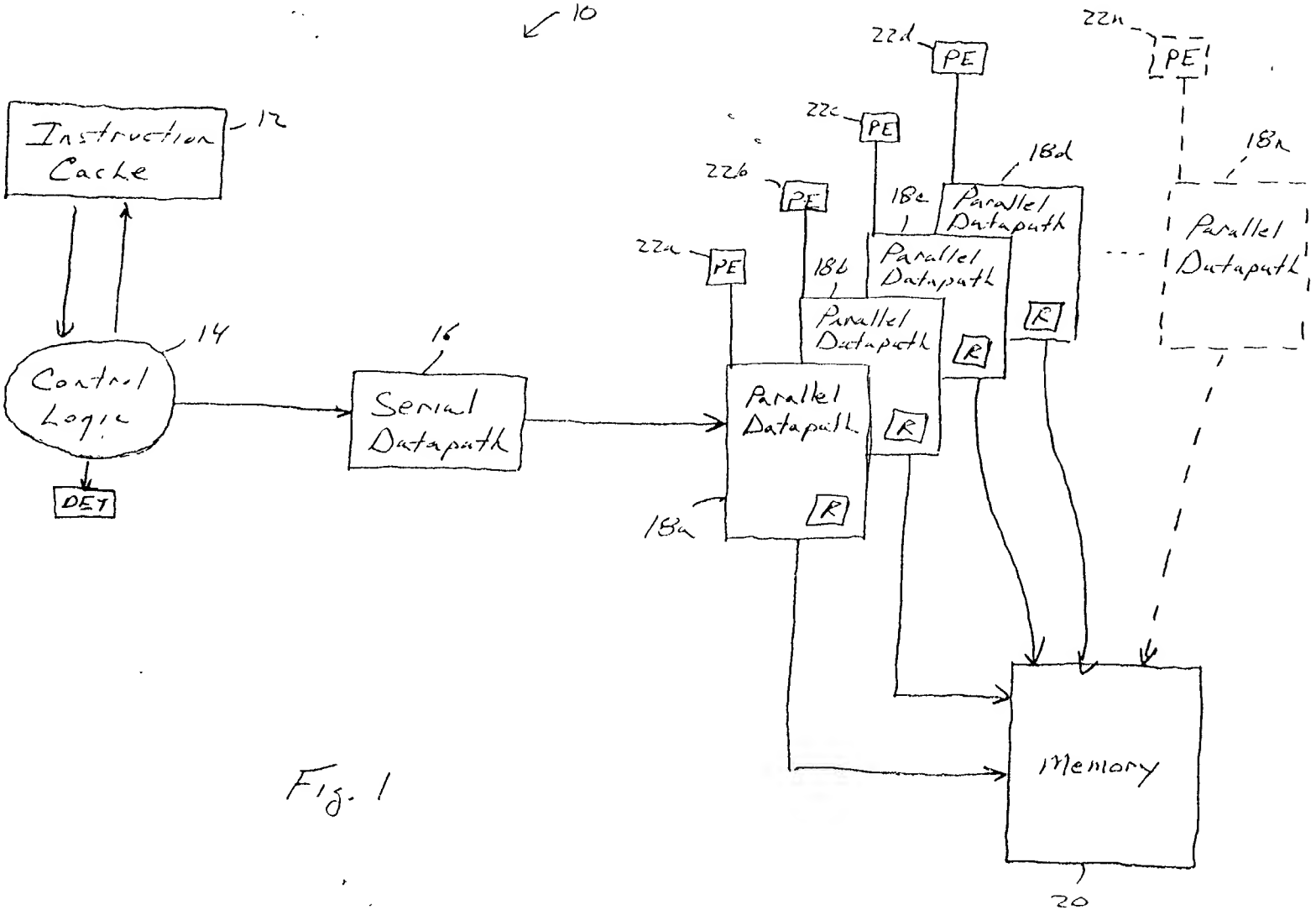

Fig. 1

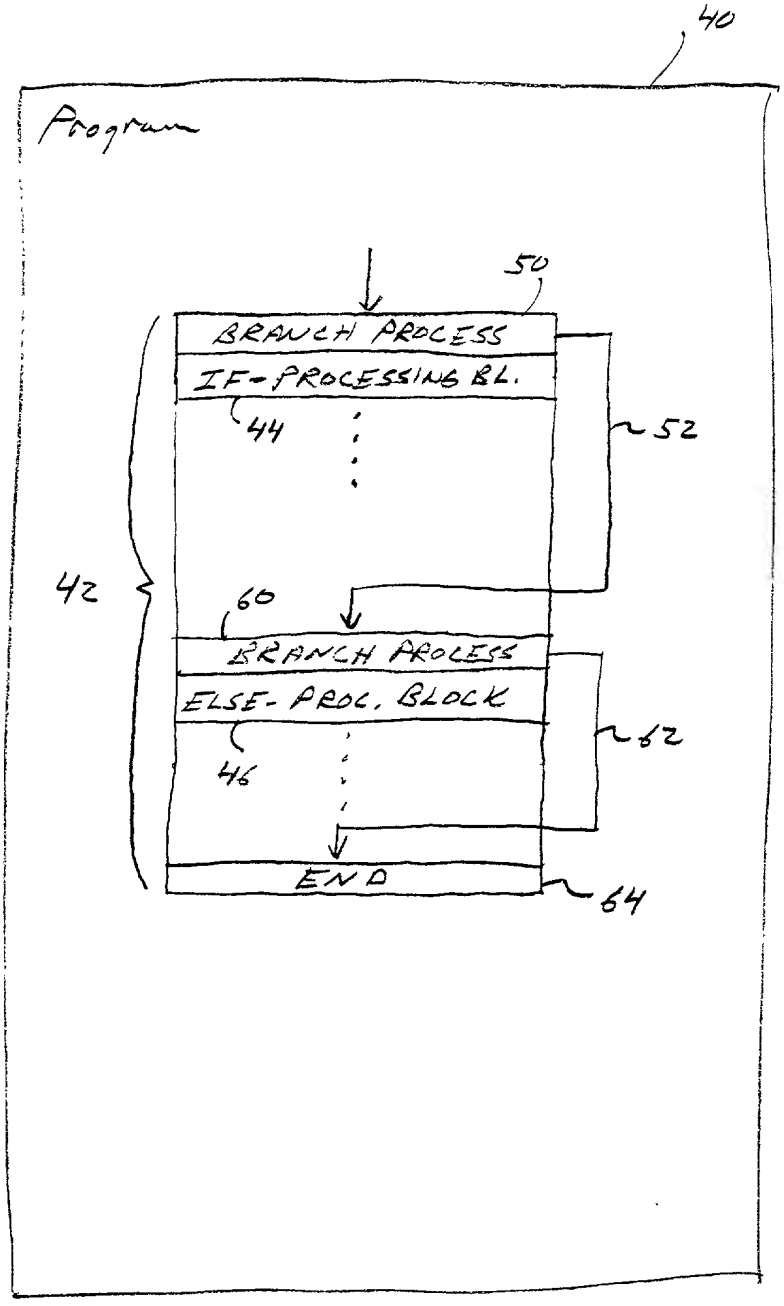
40
Program
50
BRANCH PROCESS
IF-PROCESSING BL.
44
52
42
60
BRANCH PROCESS
ELSE-PROC. BLOCK
62
46
END
64

Fig. 2

Attorney's Docket No.: 12407-004001
Client's Ref. No.:

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled BRANCH HANDLING FOR SINGLE INSTRUCTION MULTIPLE DATAPATH PROCESSOR ARCHITECTURES, the specification of which:

[X] is attached hereto.
[] was filed on _ as Application Serial No. _ and was amended on _____.
[] was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Peter J. Devlin, Reg. No. 31,753
Denis G. Maloney, Reg. No. 29,670
Gary A. Walpert, Reg. No. 26,098
Cathy Peterson, Reg. No. 41,249

Address all telephone calls to PETER J. DEVLIN at telephone number (617) 542-5070.

Address all correspondence to PETER J. DEVLIN at:

FISH & RICHARDSON P.C.
225 Franklin Street
Boston, MA 02110-2804

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Full Name of Inventor: JOHN REDFORD

Inventor's Signature: _____ Date: _____
Residence Address: 15 Saville Street, Cambridge, MA 02138
Citizenship: U.S.
Post Office Address: Same as above